TOKYO ELECTRON

SEMICON Taiwan 2026 IR Tech Talk

September 2, 2026

Investor Relations
Tokyo Electron

IR Tech Talk

Jack Ishida

Senior Executive
Chief Operating Officer
Tokyo Electron

Tatsuya Nagakubo

Executive Advisor
Tokyo Electron

Chairman
Tokyo Electron Taiwan

Peter Loewenhardt

General Manager,
Technology Strategy
Tokyo Electron

Sam Nakama

President
Tokyo Electron Taiwan

Ray Huang

Moderator

Account Sales Director
Tokyo Electron Taiwan

Agenda

- Opening Remarks
  Tatsuya Nagakubo, Executive Advisor, Tokyo Electron / Chairman, Tokyo Electron Taiwan
- TEL's Growth Strategy for Digital & Green Future
  Jack Ishida, Chief Operating Officer, Tokyo Electron
- TEL Innovations Supporting the AI Era
  Peter Lowenhardt, General Manager, Technology Strategy, Tokyo Electron
- Q&A Session
  Moderator: Ray Huang, Account Director, Tokyo Electron Taiwan
- Closing Remarks
  Sam Nakama, President, Tokyo Electron Taiwan

Opening Remarks

Tatsuya Nagakubo

Executive Advisor, Tokyo Electron
Chairman, Tokyo Electron Taiwan

Opening Remarks

TEL is committed to:

- Advancing technology leadership
- Strengthening local partnership
- Growing together with customers over the long term
- Investing in people

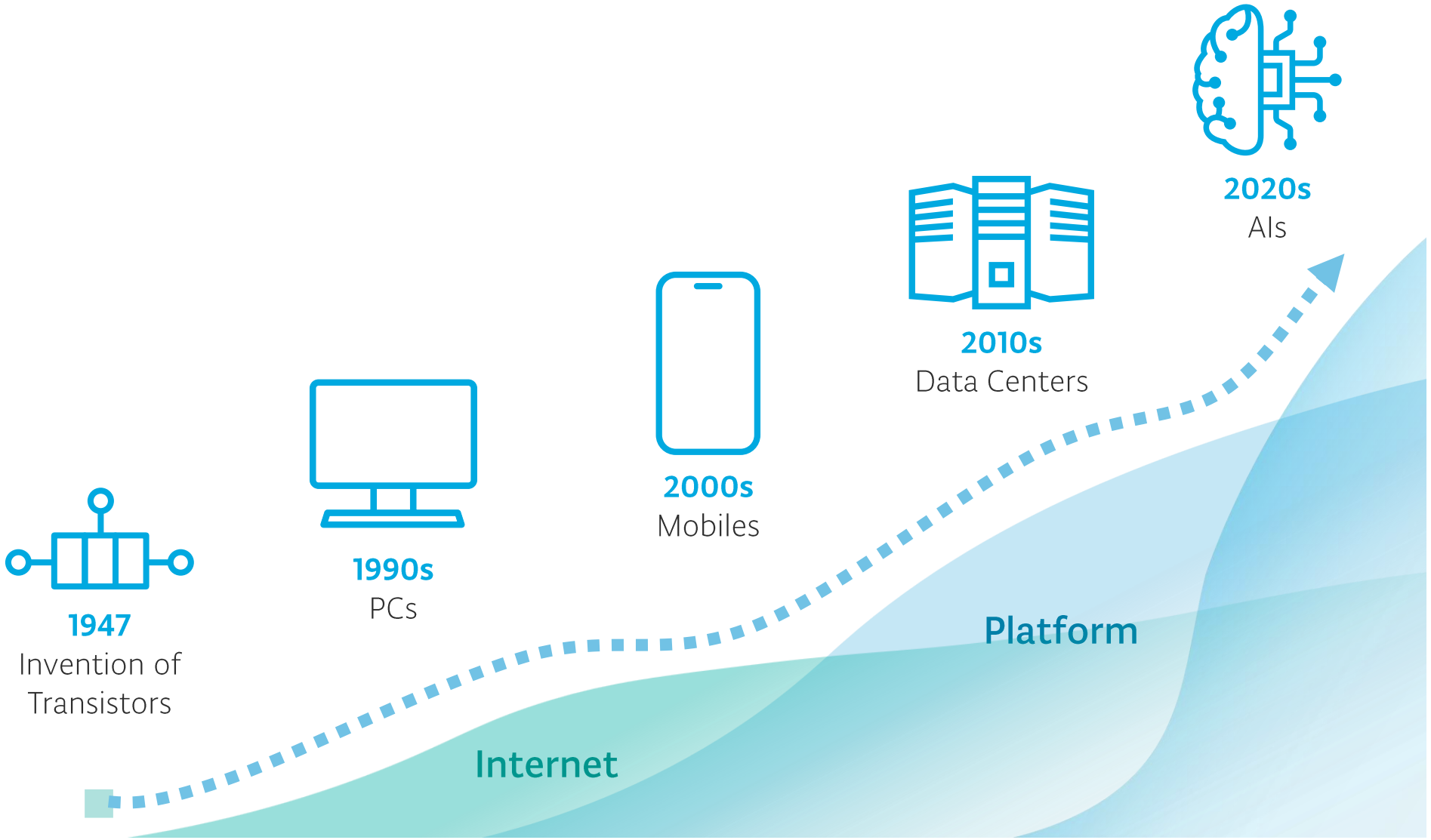
Taiwan is one of the world's most important semiconductor innovation hubs

TEL's Growth Strategy for Digital & Green Future

Jack Ishida

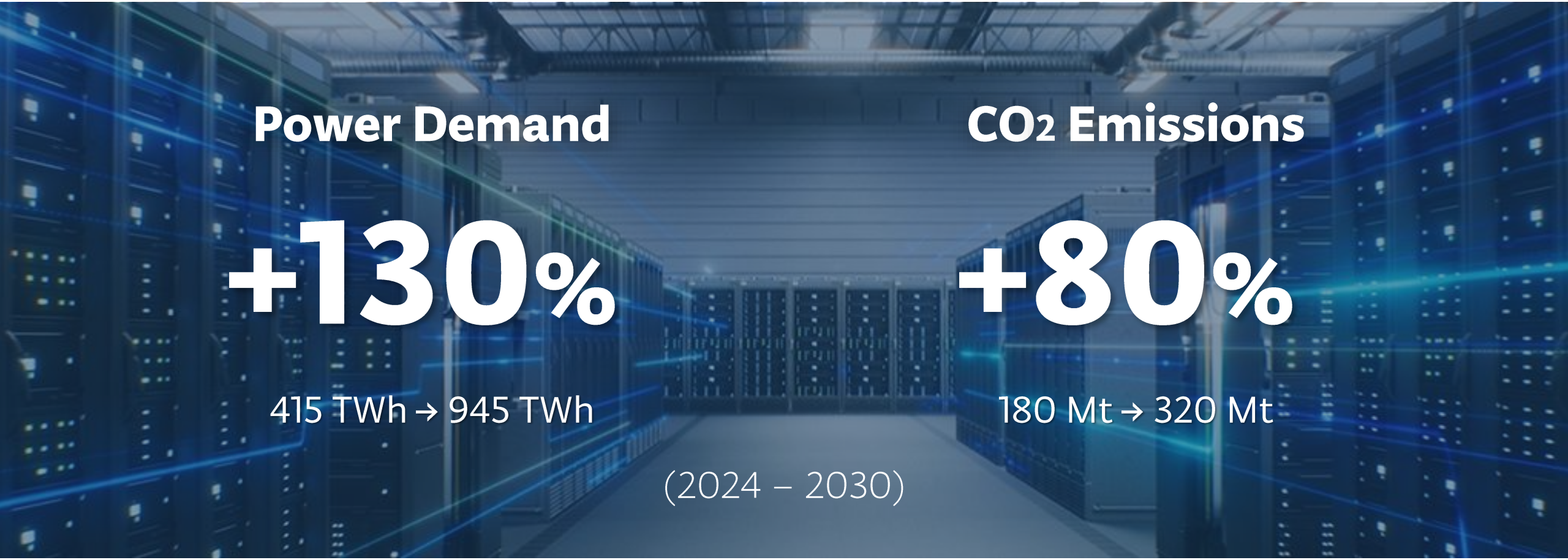
Chief Operating Officer
Tokyo Electron

History of the ICT Industry



The Future Led by ***AI***

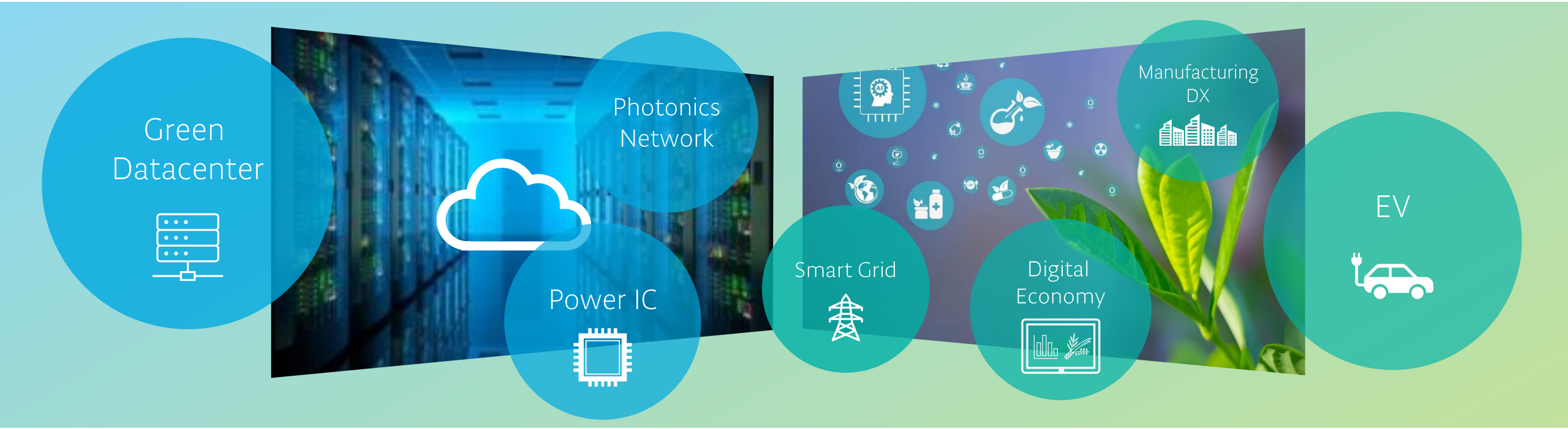
Data Centers Are Increasing Environmental Impact



Source: International Energy Agency

TEL

Digital & Green



“Green of Digital” & “Green by Digital”

TEL

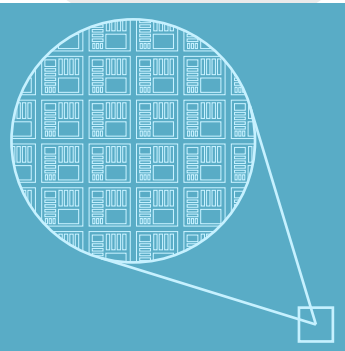
Digital & Green

Higher Speed

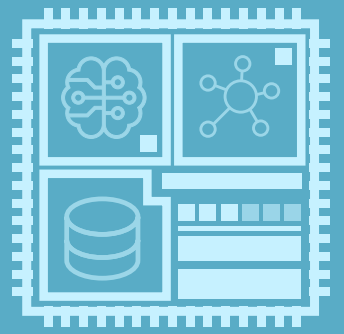
Larger Capacity

Superior Reliability

Lower Power Consumption

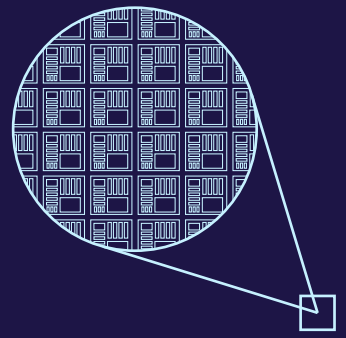


Physical Scaling

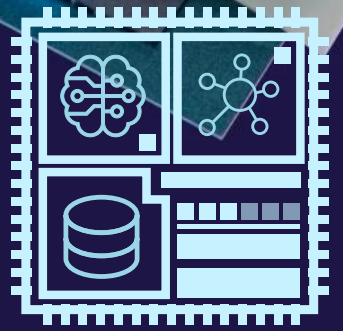


Advanced Packaging

TEL



Physical Scaling



Advanced Packaging

Unprecedented Capacity Expansion Continues

107

new fabs coming online through 2028

Source: SEMI World Fab Forecast Q325 (Sep. 2025)

Challenges for Sustainable Growth

Increase in R&D and Manufacturing Costs

- Complex device structures
- Increased process steps
- Extended development periods

Market Expansion and Fluctuations

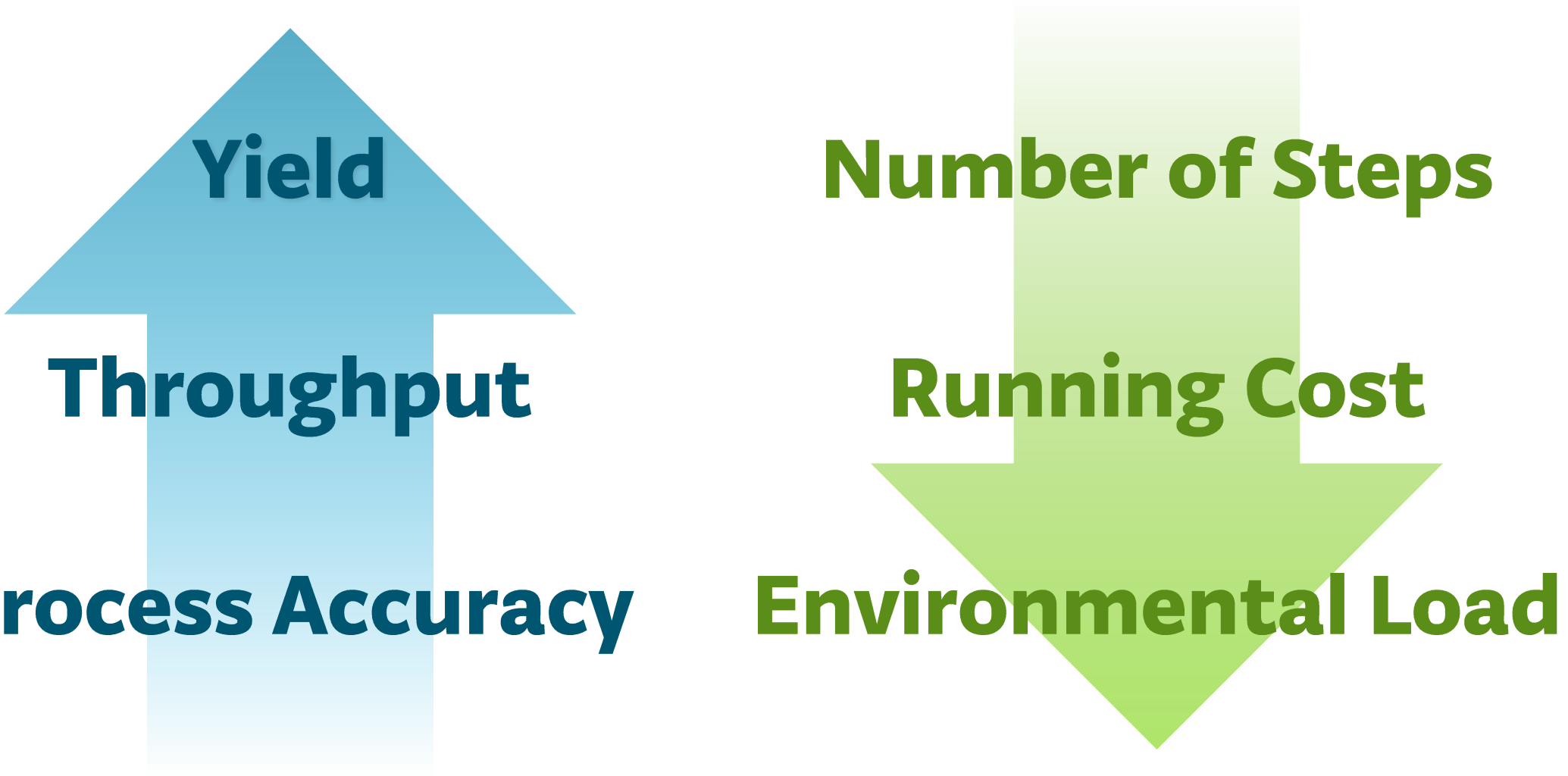
- Maximizing production capacity
- Talent War
- Industry cyclicality and External Risks

Environmental Impact

- Electricity consumption
- Water consumption
- Chemical substance regulations

As semiconductors become increasingly important and demand continues to grow, addressing key industry challenges has become more critical than ever

Growing Expectations for Equipment Manufacturers



Vision

"A company filled with dreams and vitality that contributes to technological innovation in semiconductors”

Innovation

Pursue technological innovation in semiconductors that supports the sustainable development of the world.

Profitability

Continuously create high value-added leading-edge equipment and technical services.

People

Our corporate growth is enabled by people, and our employees both create and fulfill company values Stakeholder Engagement.

Expanding Opportunities: Wide Product Portfolio

Front-end | **Advanced Packaging**

Deposition | Lithography | Etch | Cleaning | Test | 3D Integration

Batch Deposition | Semi-batch Deposition | Single Deposition | Coater/ Developer | Plasma Etch | Gas Chemical Etch | Cleaning | Prober | Wafer Bonder/ Debonder | Wafer Edge Trimming

Our broad portfolio addresses semiconductor manufacturing requirements across both Front-end and Advanced Packaging

TEL

Product Initiatives

CLEAN TRACK™ LITHIUS Pro DICE™

Chemical Consumption	Environmental Performance
50% ↓	25% ↑

Ulucus™ LX

DIW Usage	
90% ↓	Operation Steps Area Efficiency

EVAROS™

CO_2 Emission	
25% ↓	Up to 200 wafers processing capability at a time

LEXIA™ -EX

CO_2 Emission	Throughput
14% ↓	20% ↑

We are supporting high process and environmental performance


Manufacturing DX
with AI & Robotics
Epsira

Key Benefits of Epsira™

Equipment

- **Process Optimization**
  - Outcome Prediction & Feedback
  - High-Precision Control
  - Data Analytics & Improvement
- **Predictive Maintenance**
  - Condition monitoring & diagnostics
  - Early anomaly detection
  - Autonomous maintenance

AI

Epsira

Field Service

- **Delivery Enhancement**
  - Remote support
  - Robotics-enabled efficiency
- **Consistent Quality**
  - Knowledge accumulation and utilization
  - xR-enabled skill development

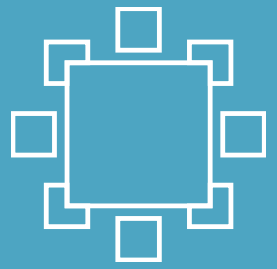
Faster Ramp-up | **Higher Yield** | **Maximum Uptime**

Accelerating Semiconductor Innovation for

Digital & Green

Investment for Future Growth (FY2025 to FY2029)

R&D Investment



1.5
Trillion Yen

Capex

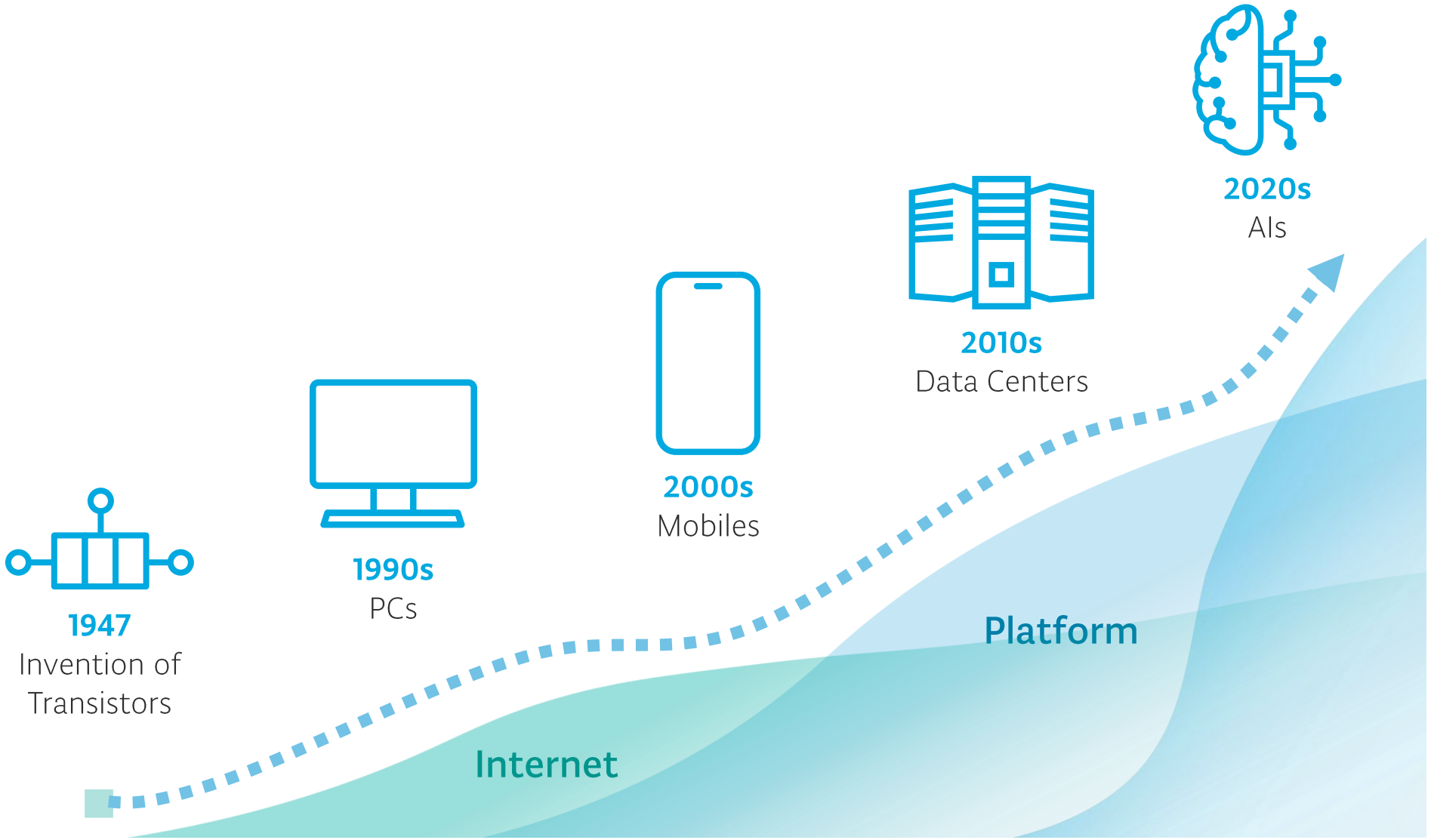
700
Billion Yen

Recruitment

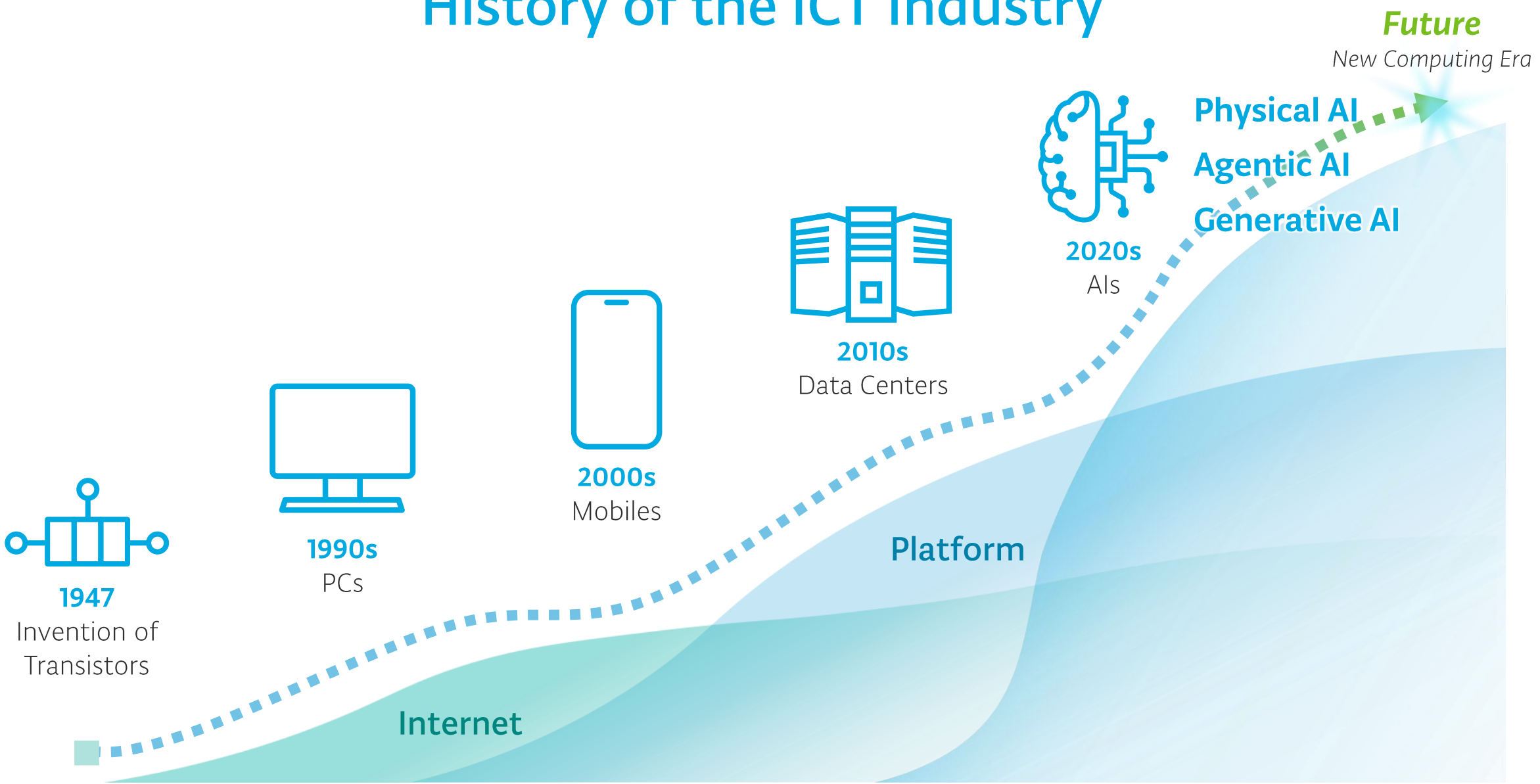
10,000
People
2000 people / year

Planning proactive investments for further growth

History of the ICT Industry



History of the ICT Industry



Semiconductors Are The Future

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TEL Innovations Supporting the AI Era

Peter Loewenhardt

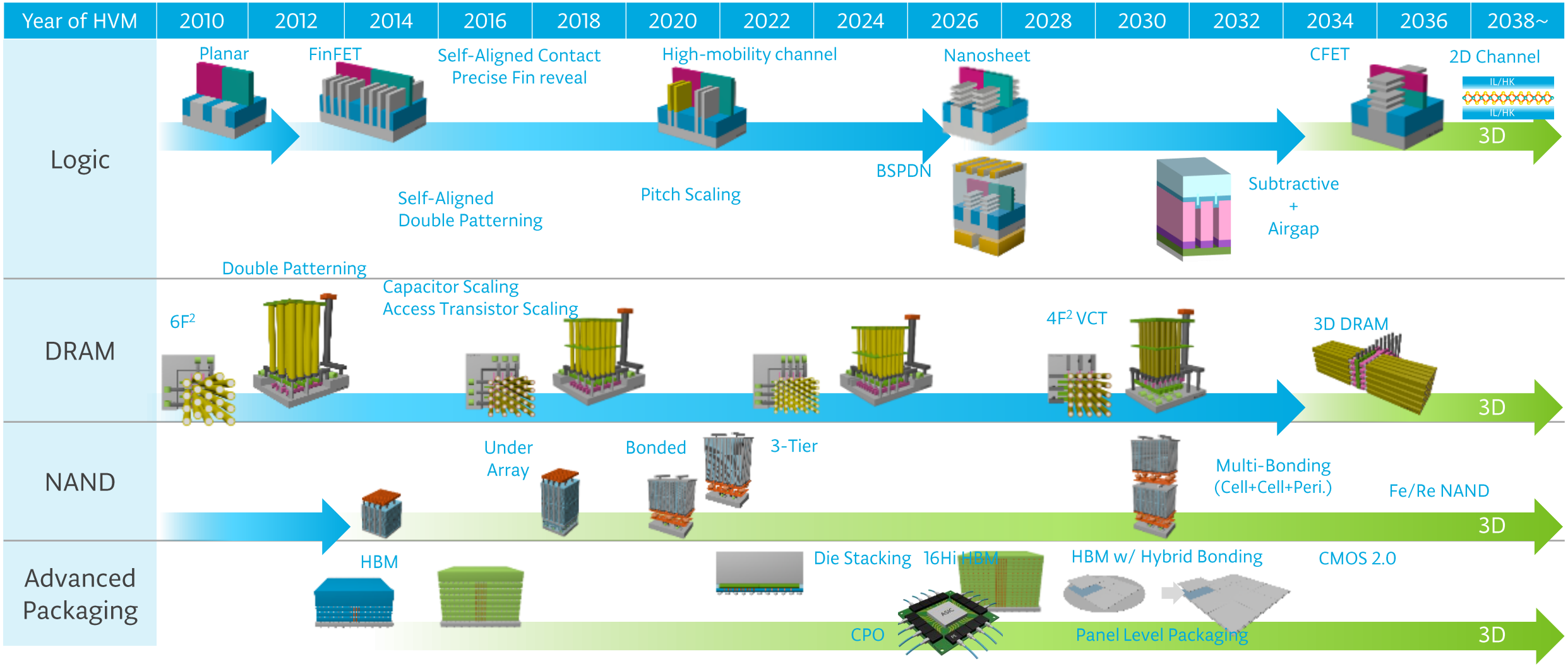
General Manager, Technology Strategy
Tokyo Electron

Roadmaps & Technology Challenges: Logic & Memory

Key device structure and integration technology inflections

Technology Roadmaps

Source of all drawings: TEL



TEL

Key device structure and integration technology inflections
Process Innovations

Technology Roadmaps

Source of all drawings: TEL

Year of HVM	2010	2012	2014	2016	2018	2020	2022	2024	2026	2028	2030	2032	2034	2036	2038~
Logic	Planar	FinFET		Self-Aligned Contact Precise Fin reveal Atomic Layer Etch Chemical etch		High-mobility channel SiGe epi Conformal Silicide Metal depo Bottom-up Via Fill			Nanosheet		Seamless lateral gapfill CFET HARC Etch, HAR Via Fill Vertical Patterning			2D Channel IL/HK IL/HK 3D	
	Double Patterning		Self-Aligned Double Patterning Conformal film depo		EUV	Pitch Scaling	Gas Cluster Beam Trimming	BSPDN Low-distortion bonding Backside grinding	Metal-Oxide Resist High-NA EUV		Subtractive + Airgap		Low-Rs metal depo Fine-Pitch Metal Etch Volatile material depo		
DRAM	6F² HARC Etch		Capacitor Scaling Access Transistor Scaling Conformal high-k dielectric depo			No pattern collapse High-Stiffness Bot Electrode depo		4F² VCT					3D DRAM 3D		
NAND			HARC Etch ONON Mold depo W replacement	Under Array		Bonded	3-Tier Hybrid Bonding Laser Edge Trim	New HARC Etch	New WL metal Cryo Etch		MIC/MILC Multi-Bonding (Cell+Cell+Peri.)		Fe/Re NAND 3D		
Advanced Packaging			HBM Temporary Bonding Backside grinding				Die Stacking	16Hi HBM Hybrid Bonding CPO			HBM w/ Hybrid Bonding Plasma Dicing (2-in-1) Panel Level Packaging Equipment for larger package size		CMOS 2.0 W2W hybrid bonding 3D		

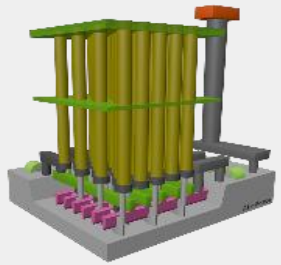
Device inflections have been, and will continue to be, driven by process innovation

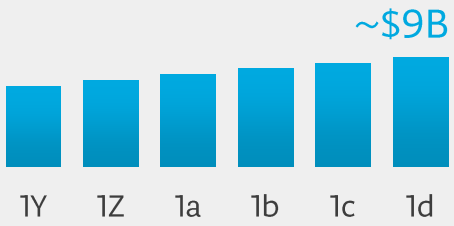
TEL

Raising Added-value in SPE (Semiconductor Production Equipment)

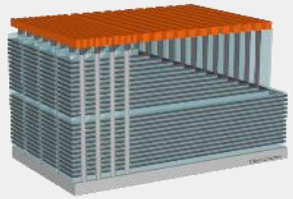
WFE investment (100k WSPM*, Greenfield / TEL estimates)

DRAM

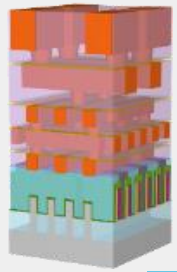


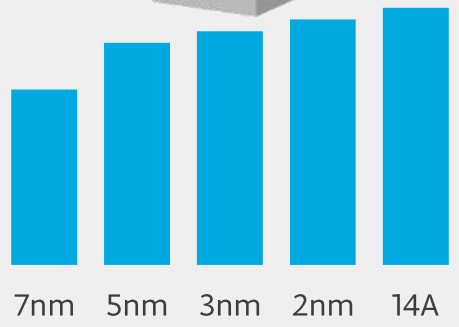


3D NAND



Logic





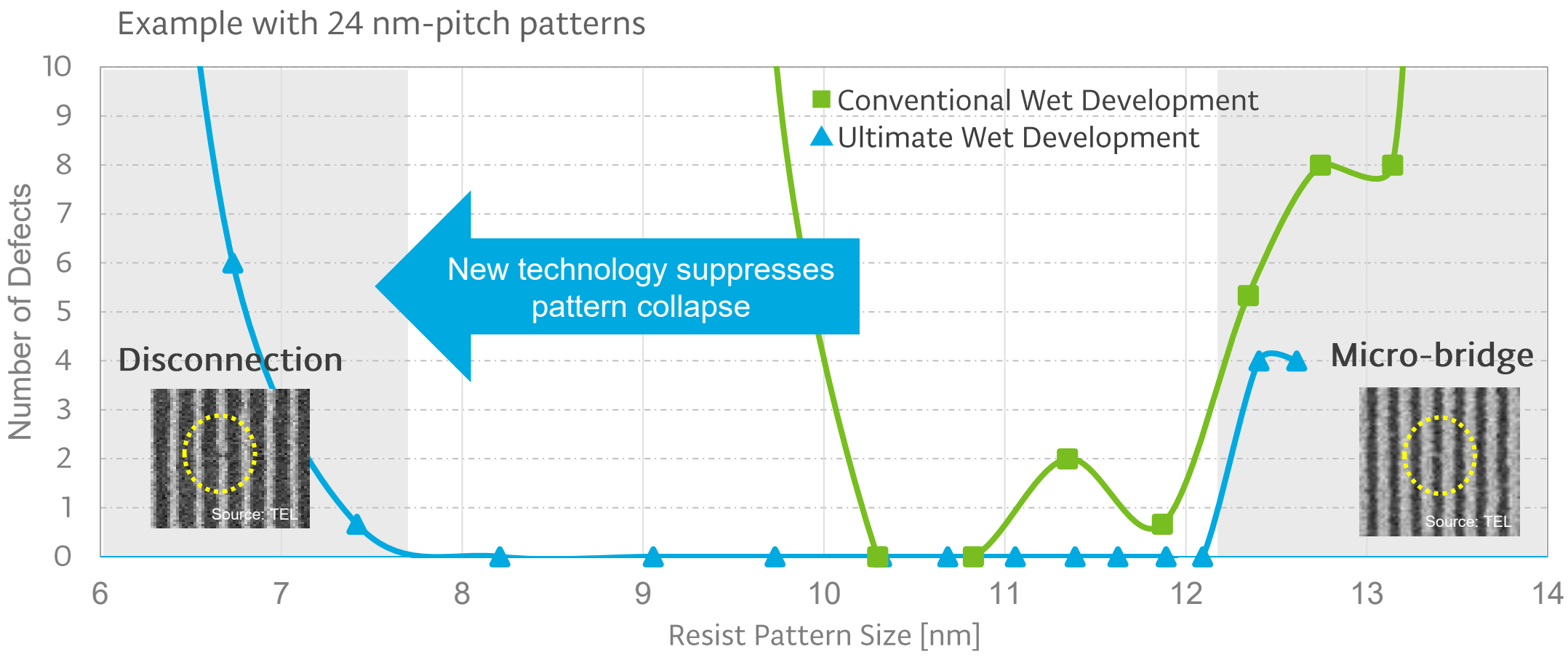
Expanding business opportunities for SPE manufacturers on arrival of new applications and rising level of technological difficulty

* WSPM: Wafer starts per month

TEL R&D Roadmap Activities

Patterning

Example of MOR Process: The Ultimate Wet Development



The Ultimate Development technology enables the suppression of pattern collapse

Example of MOR Solution: The Ultimate Wet Development

*1 Based on internal information and development targets
*2 Based on results of developing 24 nm-pitch lines

	Ultimate Wet Development Technology	Conventional Wet Technology	Alternative Technology
Base Technology	Coater/Developer	Coater/Developer	Etch
Process Ambient	Atmospheric	Atmospheric	Vacuum
Reaction	Chemicals	Chemicals	Corrosive Gas
Throughput*1	4x	4x	1x
Chemical Consumption*1	50% (vs. conventional)	100 %	N/A (uses gas) exhaust processed in combustion abatement post process
Anti-Pattern Collapse*1 Performance	< 8 nm*2	> 10 nm*2	< 8 nm*1
Footprint*1	In-Line	In-line	Additional Footprint

Evaluation of Ultimate Wet Development ongoing with key customers, with emphasis on productivity (throughput, footprint, maintainability, utilize existing facilities)

CLEAN TRACK™ LITHIUS Pro DICE™

Coater/Developer

Features

- High-productivity and High-environment performance by maximizing footprint efficiency
- Reduced coater-related defects and chemical usage with new resist dispense system
- Reduced SU and LT through autonomous control
- Enhanced system condition monitoring

Applications

- All lithography processes, including High-TP exposure inline
- Advanced EUV processes, including High-NA EUV

CLEAN TRACK™ LITHIUS Pro DICE™

LITHIUS Pro DICE™ offers world-class productivity and superior defect control technology with enhanced data collection and processing capabilities

Chemical Consumption

50% ↓

Cost savings caused by reduced flawed resist coating

Environmental Performance

25% ↑

Industry-fastest processing speeds with maximized footprint

*compared to previous models

For a wide range of applications, including high-NA EUV and DUV processes

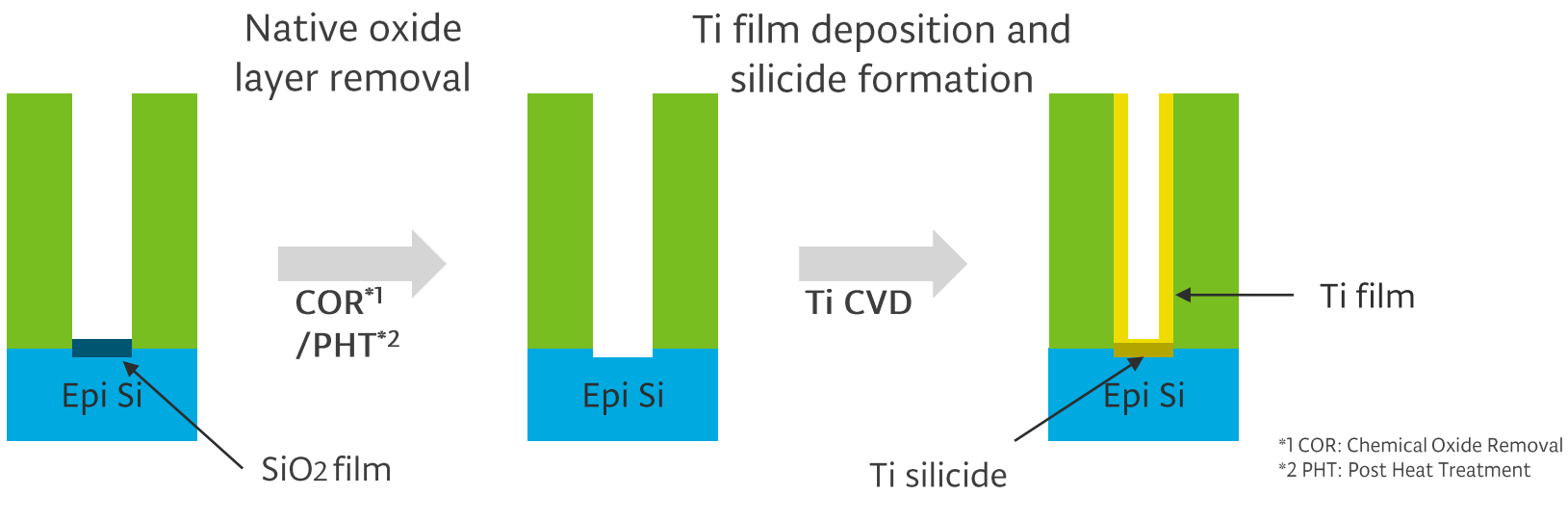
TEL

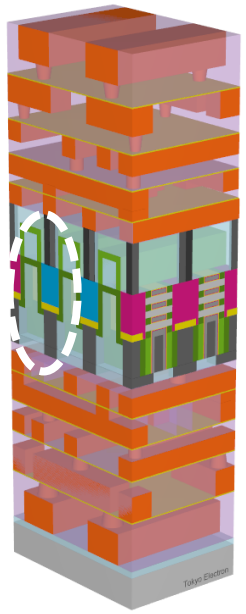
Deposition

Episode™ 1: Contact Formation Process

Source of all drawings: TEL

- Example of process flow



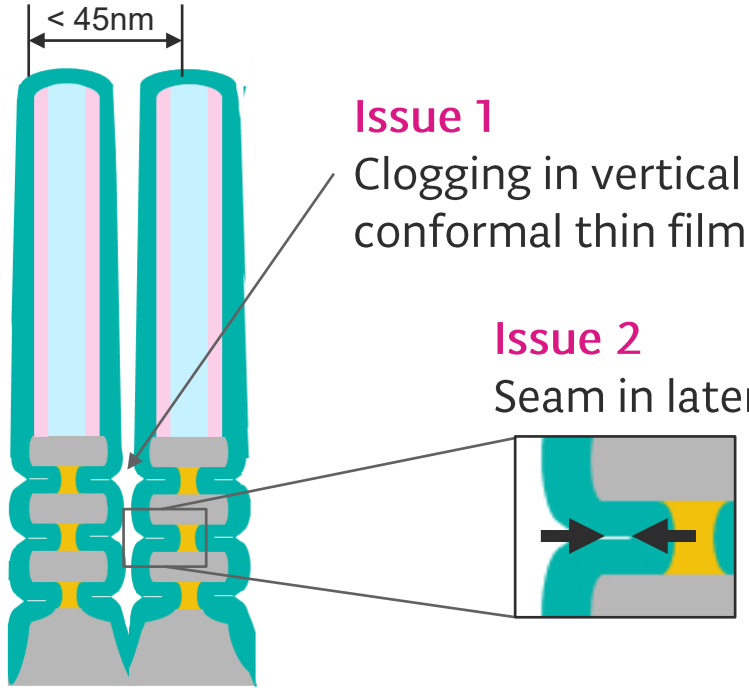


Multiple types of process modules are equipped on a high-vacuum transfer module, and low-resistance contacts are achieved by sequentially processing native oxide layer removal and metal film formation

GAA: Inner Spacer Formation - Lateral Gapfill

Source of all drawings: TEL

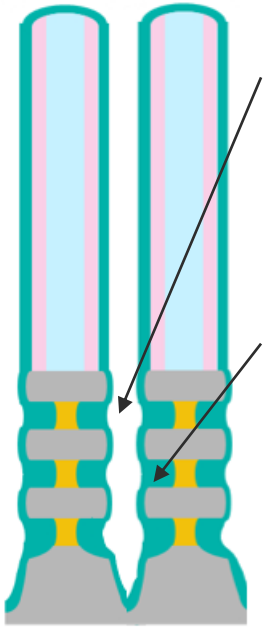
- Issues :
  Leak due to dielectric breakdown due to etching



Issue 1
Clogging in vertical gap due to conformal thin film deposition

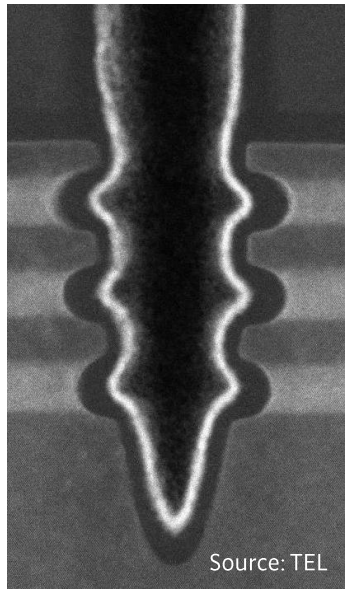
Issue 2
Seam in lateral gap

- Solutions :
  Improve lateral gapfill performance



Solution 1
Thinner film deposition on the side walls

Solution 2
Seamless gapfill in lateral gap



Realized seamless lateral gapfill using a unique thin film deposition technique and laterally uniform film modification using a newly developed high-density plasma

Wet Processing

Single Wafer Cleaning Strategy

Source of all drawings: TEL

Single Wafer Cleaning

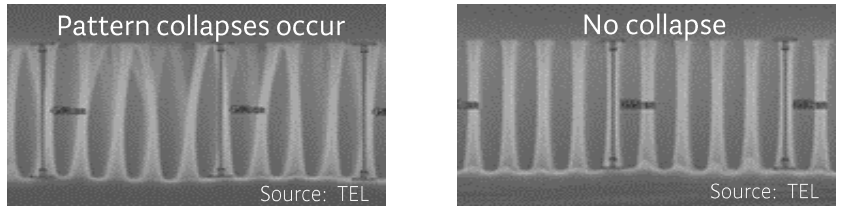
- Bevel wet etch
  - Expect annual market growth rate of around 10%
  - Contribute to improving customers' yields.
    Maintain a high market share by differentiating through performance in precisely removing film from the outer part of the wafer
- Prevent pattern collapse
  Expand market share by TEL original technology to reduce collapse of high aspect ratio pattern
- Metal etch
  Launched new dedicated SPM chambers for controlling selectivity for metal in order to solve reduced yield issues caused by dry etch damage and residue

Without bevel wet etch

With bevel wet etch

Conventional drying technology

New drying technology



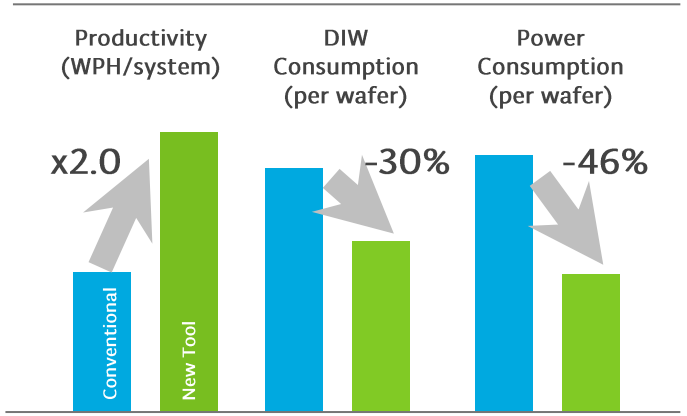
Metal etch process

Development of Cleaning Systems

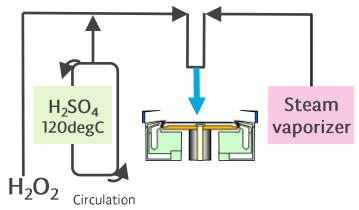
Source of all drawings: TEL

High Productivity Wet Bench (EXPEDIUS™-R)

Industry's first large-batch process (increased wafer counts)



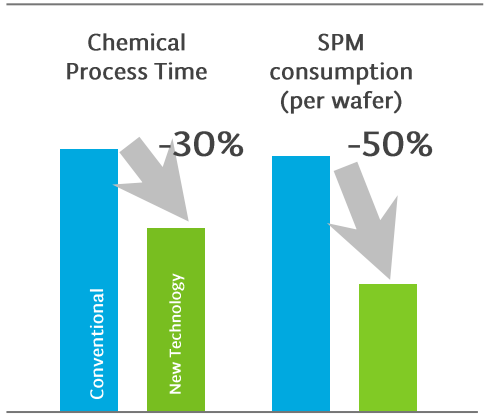
SPM*1 Vapor Technology (CELLESTA™ Pro VP)



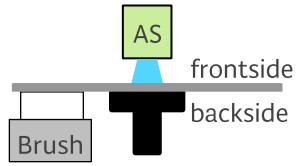
CELLESTA™ Pro VP schematic

Enabled higher temperature process due to a more effective rection by adding water vapor to chemicals

*1 SPM: Sulfuric Acid and Hydrogen Peroxide Mixture

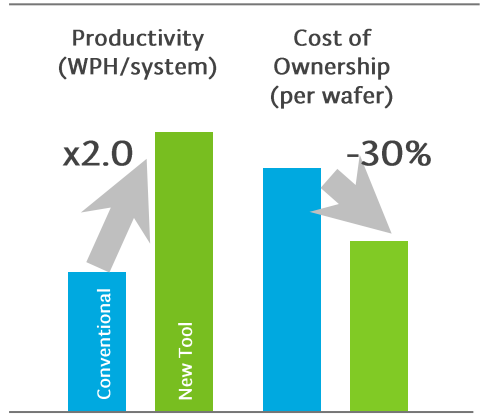


Simultaneous Scrubber (CELLESTA™ MS2)



A tool enabling AS*2 process on wafer frontside and physical brushing process on wafer backside simultaneously in a single chamber

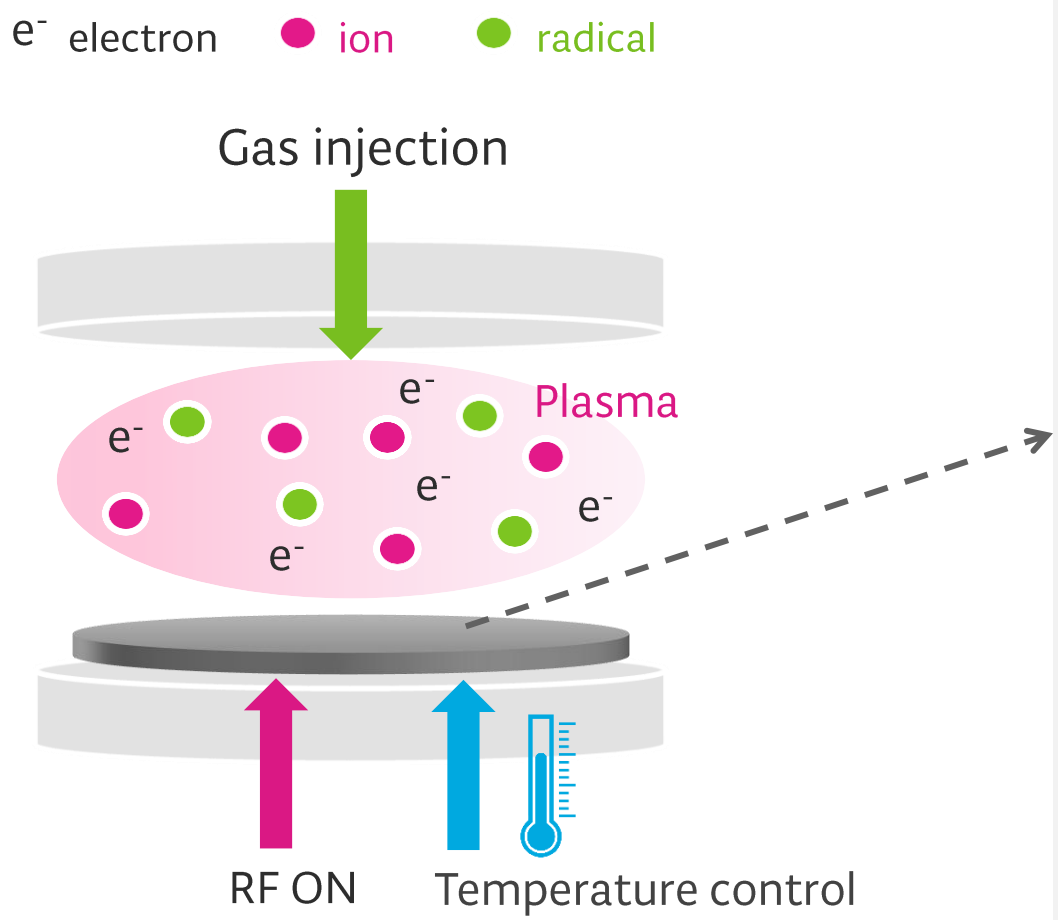
*2 AS: Atomized Spray



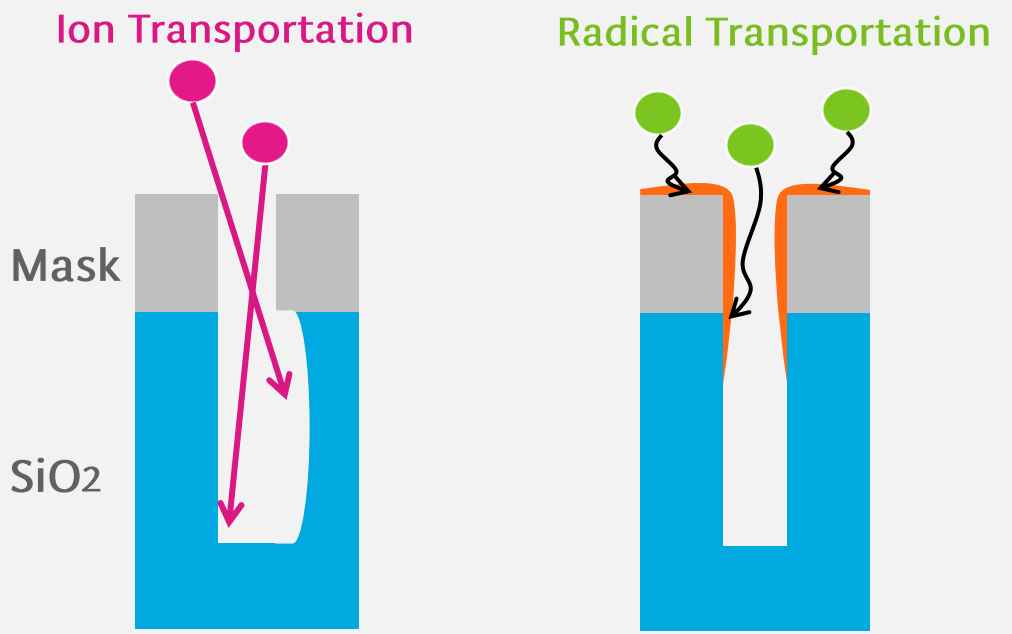
Etching (Plasma and Chemical)

Overview of Anisotropic Etching Key Parameters

Source of all drawings: TEL



Key Parameters for Etch Controllability



- Ion energy
- Ion incident angle

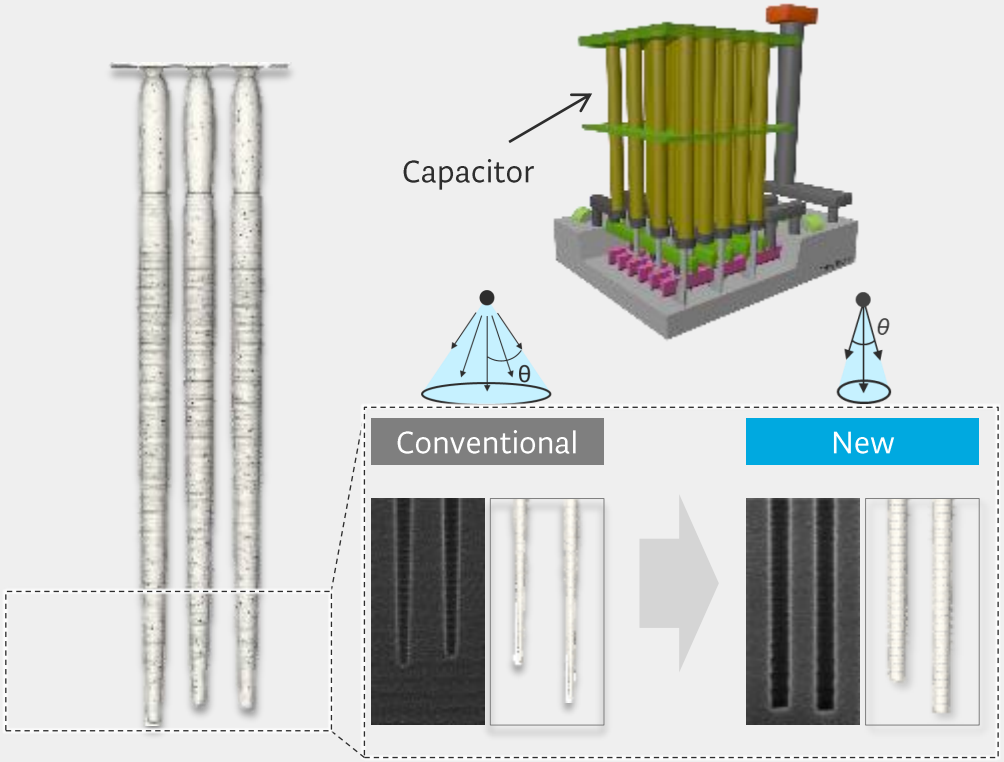
- Gas species
- Wafer temperature

TEL

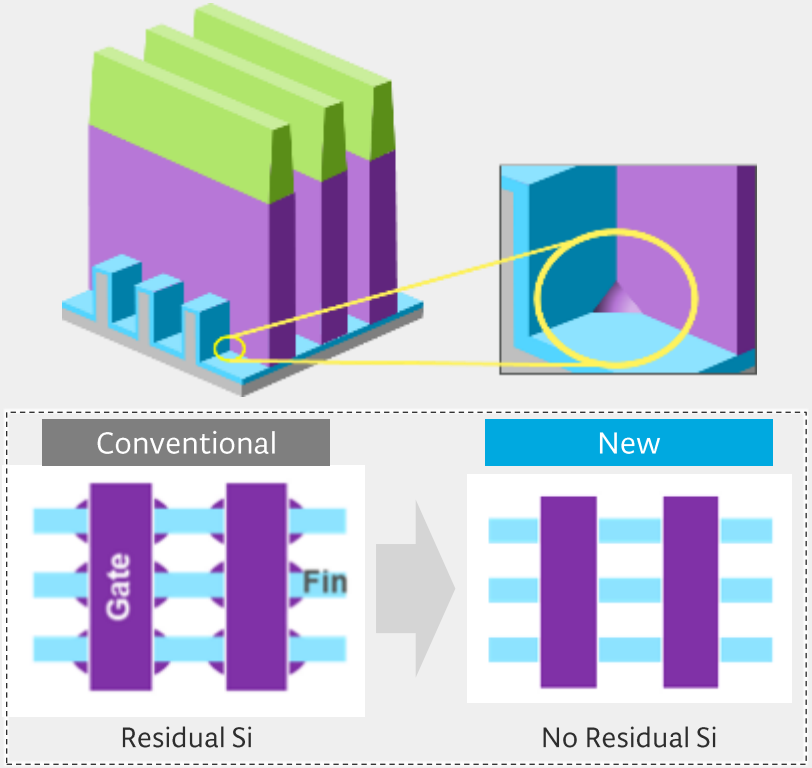
Future of New Plasma Etch Technologies (Anisotropic)

Source of all drawings: TEL

DRAM: Capacitor SiO_2 Etch



Logic: Gate Silicon Etch



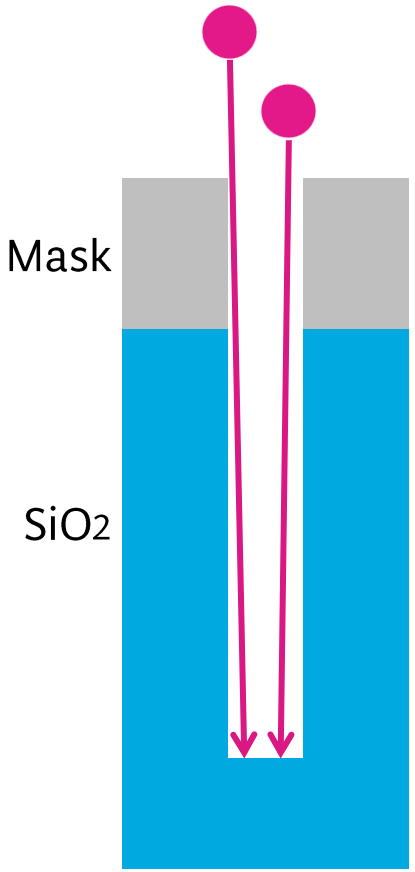
New technologies created through the development of ideal etching process development, will be applied to a variety of critical processes

Our Unique Technology 1: HERB™

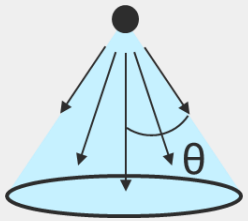
(HERB™: High Efficiency Rectangular Bias™)

Source of all drawings: TEL

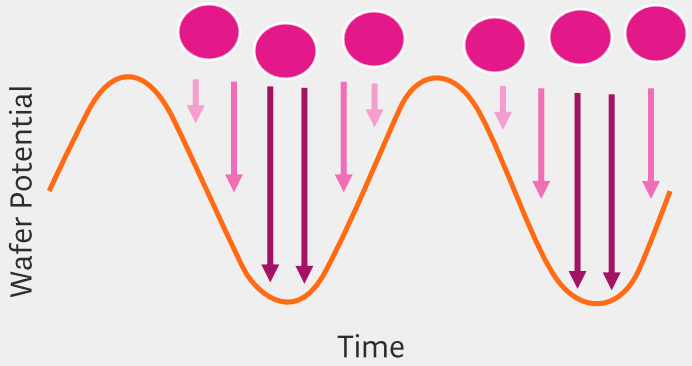
Ion transportation



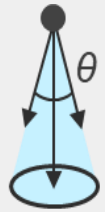
Conventional Technology (Sine wave)



The force attracting ions varies
→ incident angle varies

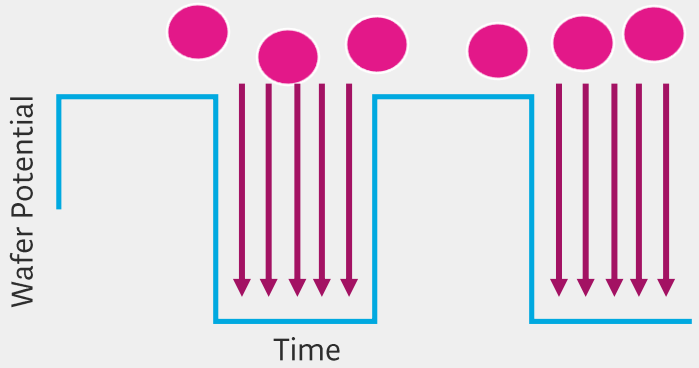


Novel Technology (HERB™)



Force attracting ions are strong and consistent

→ incidence angle becomes perpendicular



What happens when it gets cold, really cold?
My personal experience . . .

Where I grew up:

Regina, Saskatchewan, Canada

December 2019

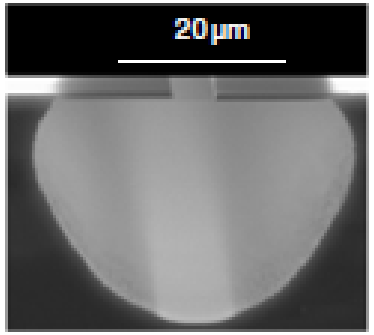
Below ~ -30°C
many common materials change behavior

Source: personal photos

Background: Cryo-Etch Potential on HAR Etching

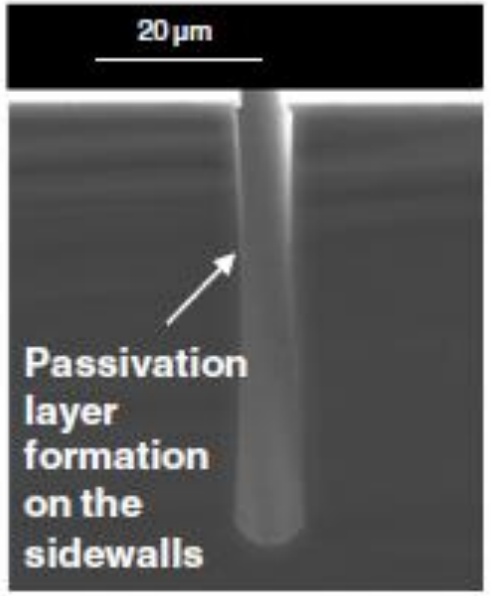
Temperature Dependency on Si etching profile

+ 30°C



SF_6/O_2 plasma

- 110°C



High efficiency radical transport
⇒ Faster etch rate

R Dussart, M Boufnichel et al. J. Phys. D: Appl. Phys. 47 (2014) 123001 (27pp)

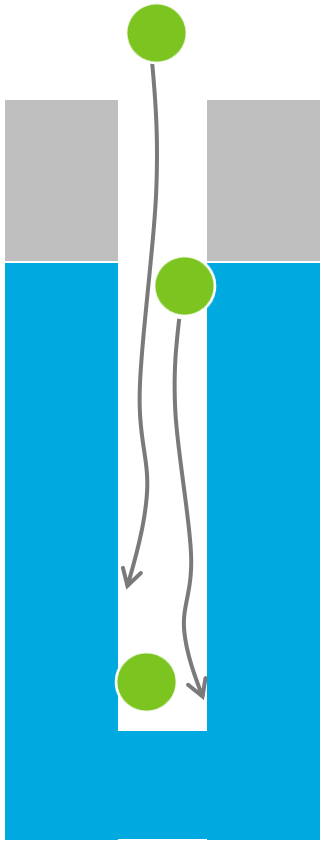
Low temperature has good potential for HAR etching

Our Unique Technology 2: PHastIE™

(PHastIE™: Phosphorus + Hydrogen based "Fast" Ion Etch™)

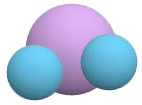
Source of all drawings: TEL

Radical transportation



Conventional Technology

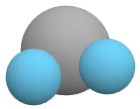
(CFx + Room Temp.)

CFx 

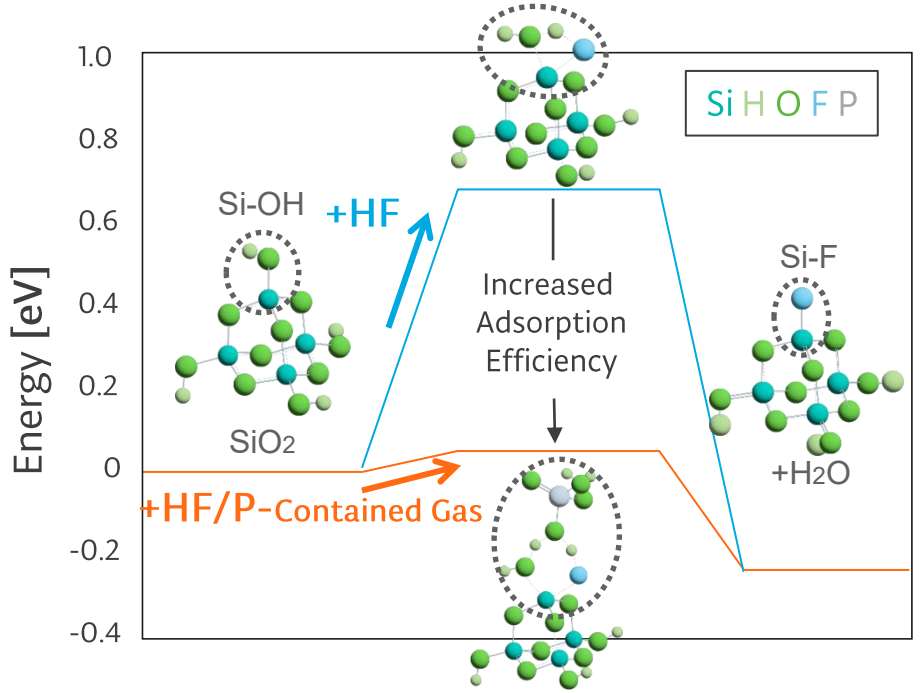
CFx tends to polymerize/adsorb easily
Hinders transportation when accumulated at top

Novel Technology

(PHastIE™)

HF  PFx 

Resolved the issue with novel gas
Achieved high etch rate in combination with low temp

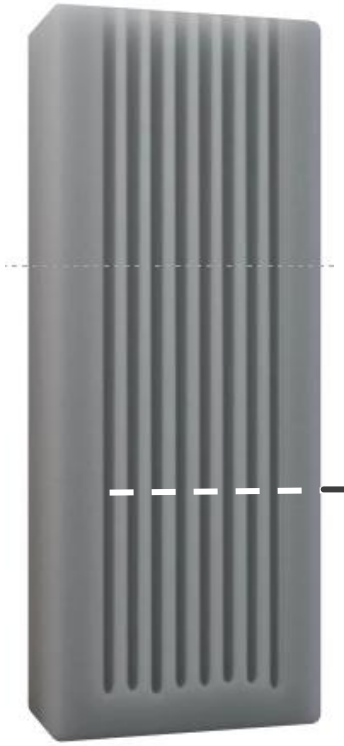


TEL

Novel Cryogenic HARC Etch

Source of all drawings: TEL

Cryogenic Process



Beyond

10 µm

2.5x

Faster

Plasma Control

Environmental Impact

-43%

Less Power

-83%

Less Carbon Footprint

Better process is also better for the environment

TEL

Basic Concept of Non-plasma Based Dry Etching

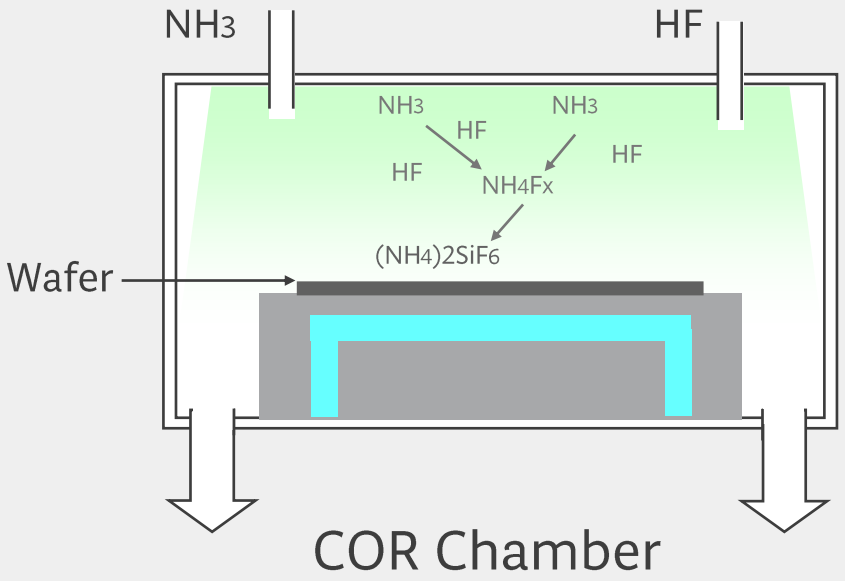
Source of all drawings: TEL

Step 1: Low Temperature Process

Chemical oxide removal (COR)

$SiO_2+4HF+4NH_3 \rightarrow SiF_4+2H_2O+4NH_3$

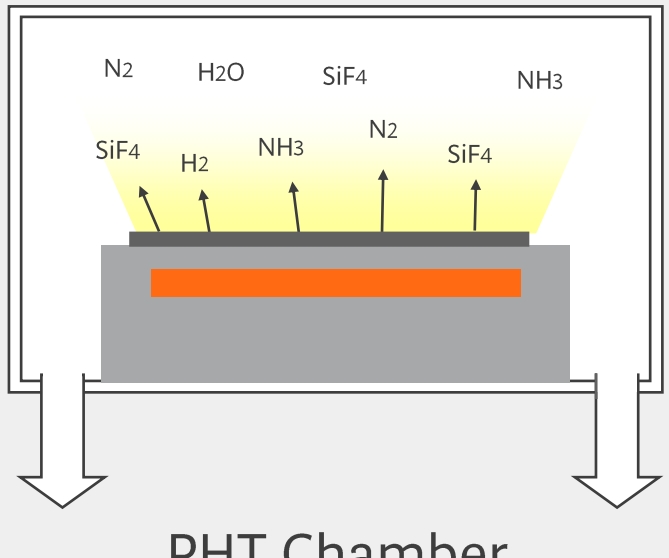
$SiF_4+2NH_2+2HF \rightarrow (NH_4)2SiF_6$



Step 2: High Temperature Process

Post heating treatment (PHT)

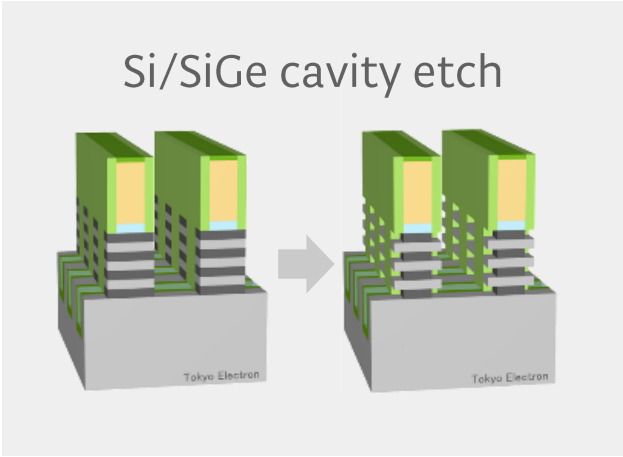
$(NH_4)2SiF_6 \rightarrow SiF_4+2NH_3+2HF$

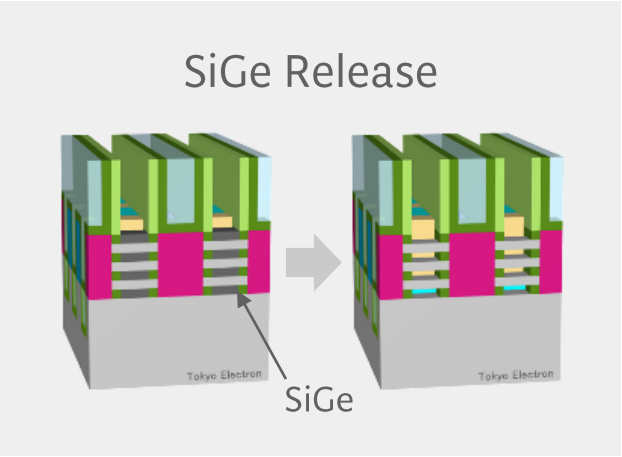


GAA NanoSheet Etch No Plasma (Isotropic)

Nano Sheet process challenges:

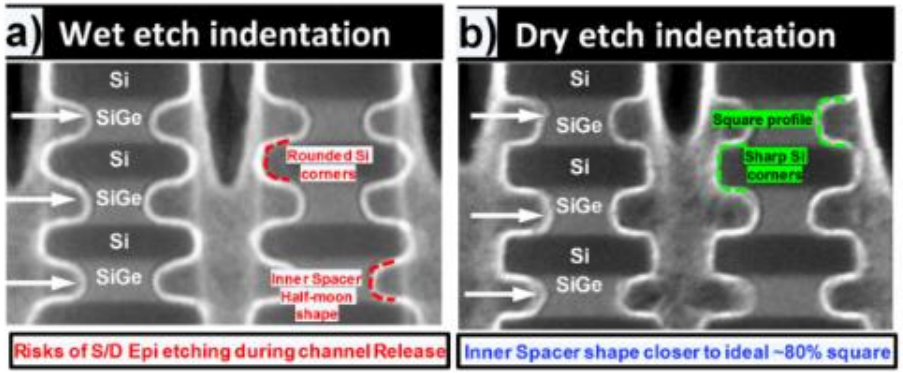
- Uniformity in rectangle shape
- Mitigation of roughness/residue on patterned surface





TEL's initiative: Gas chemical etch

- High etch selectivity
- High uniformity
- Residue removal/decreased roughness



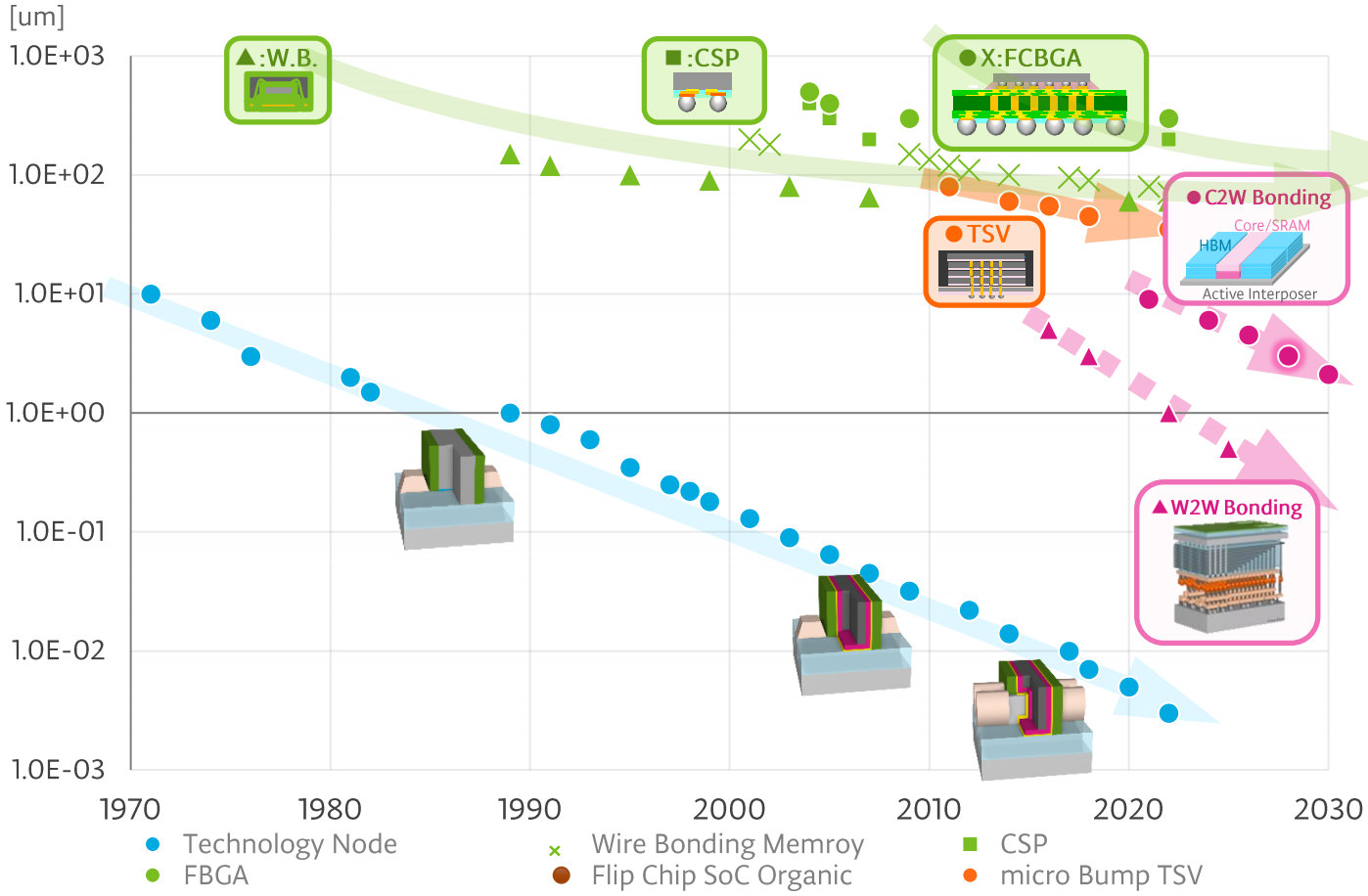
Source: N. Loubet, et al., IBM, TEL Technology Center, America (IEDM2019)

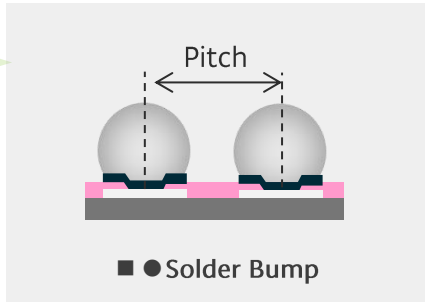
Leveraging the advantages of gas chemical etch to contribute to leading-edge processes

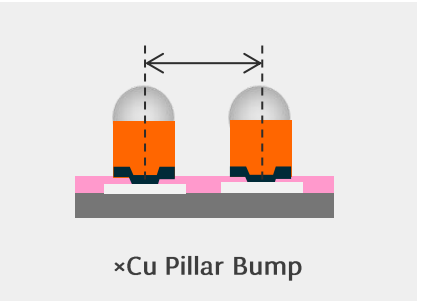
Advanced Packaging

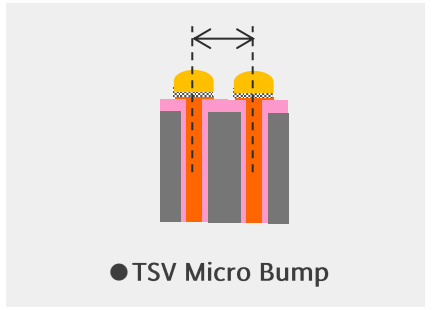
Semiconductor Technology Node and Bump Pitch

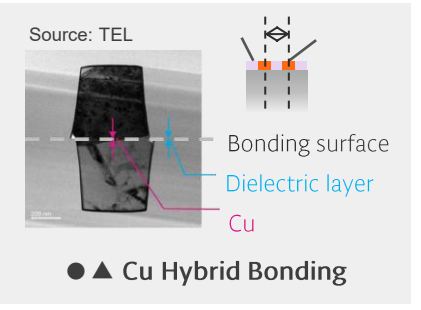
Source of all drawings: TEL











Wafer Bonding

Introduction of wafer bonding technology accelerates further reduction of pitch

3DI / Test Business Expands Opportunities for HPC/AI Device

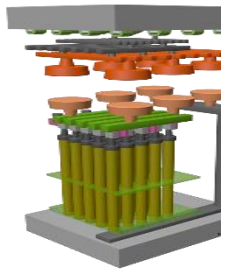
Source of all drawings: TEL

Frontend Process

Device Manufacturing

BSPDN*1

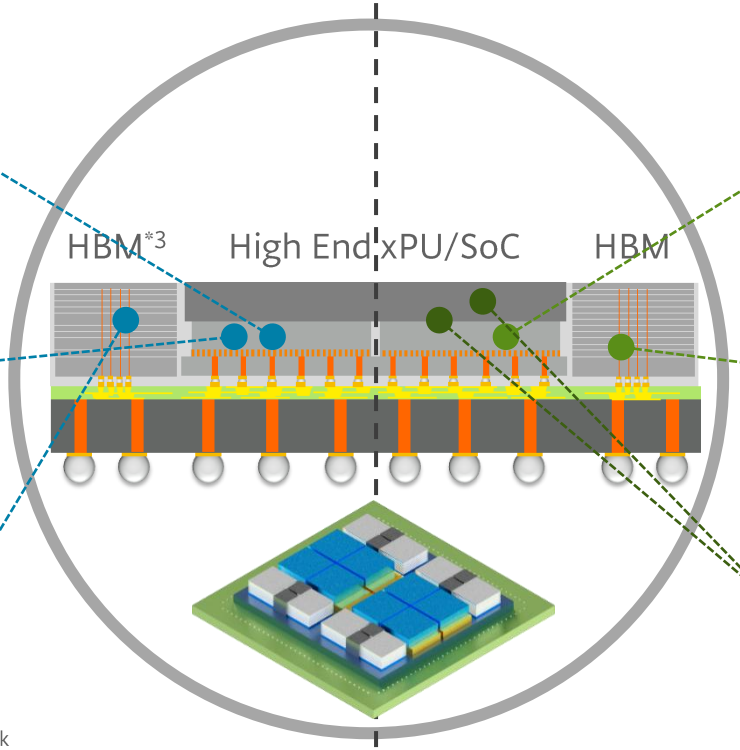
CFET*2



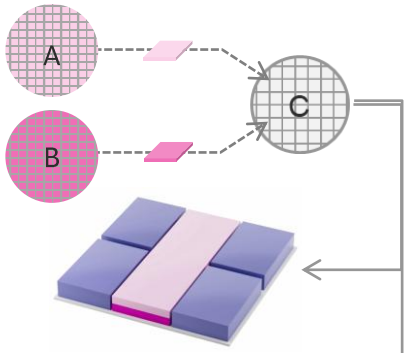
DRAM

Advanced Packaging

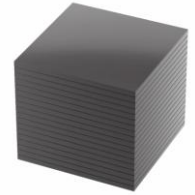
Assembly after Dicing/Singulation



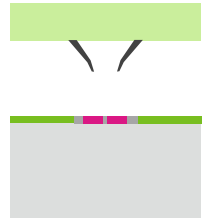
3DIC



Stack Memory



Die Test for KGD*4



*1 BSPDN: Back Side Power Delivery Network
*2 CFET: Complementary Field Effect Transistor
*3 HBM: High Bandwidth Memory
*4 KGD: Known Good Die

Source of all drawings: TEL

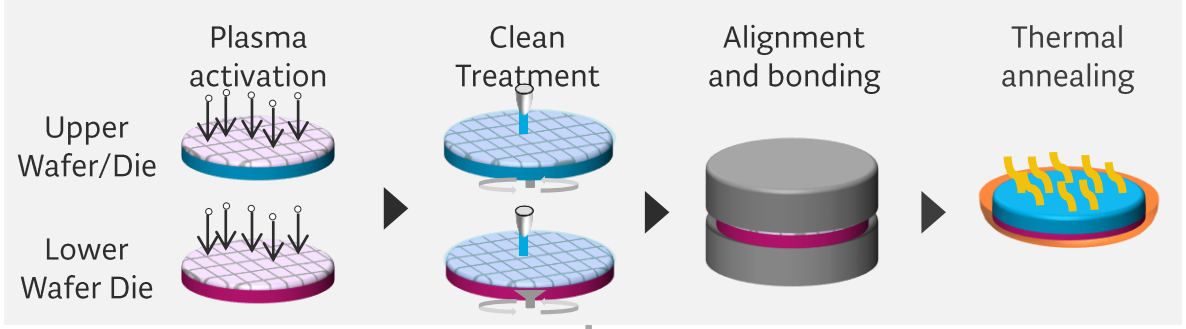
TEL

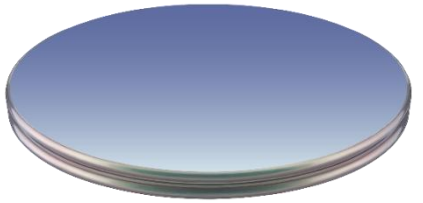
TEL's Opportunities for Bonding Technology

Source of all drawings: TEL

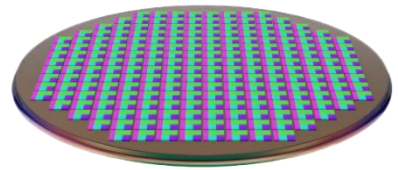
Wafer-to-Wafer Bonding

Bonding Technology





Wafer-to-Wafer Bonding



Die-to-Wafer Bonding

Benefits for Pitch scaling &
Higher speed / Lower power consumption

Frontend Process

Advanced Packaging

Source of all drawings: TEL

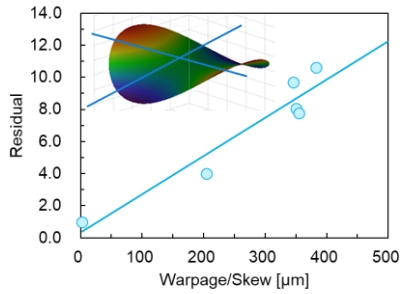
TEL

Wafer Bonder Technology Roadmap and Challenges

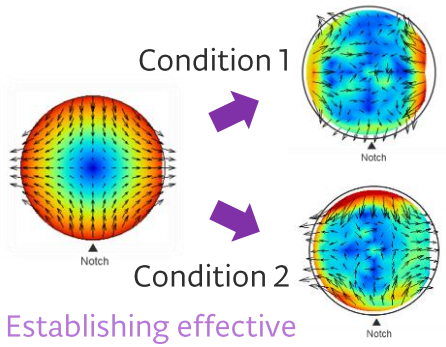
Source of all drawings: TEL

CY	2025~26	2027	2028	2029	2030~31	2032~33	2034~35	Beyond
Logic	BSPDN (2nm/18A)	(16A)	(14A)	(12A)	(10A)	(7A)	(5A) CFET	(3A)
		Distortion ≤ 4nm			Distortion ≤ 3nm		Distortion ≤ 2nm	
NAND		2-wafer-bonding				3-wafer-bonding	4-wafer-bonging	
		Wafer warpage < 500μm					Wafer warpage > 500μm	
DRAM		6F² DRAM			6F² + Peri Bonding/4F² VCT/3D DRAM			
					Distortion ≤ 3nm / DxDy < 50nm			

Wafer Warpage Challenges and Actions

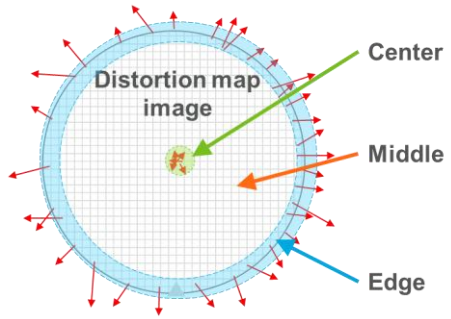


Relation between wafer warpage and residual (distortion)

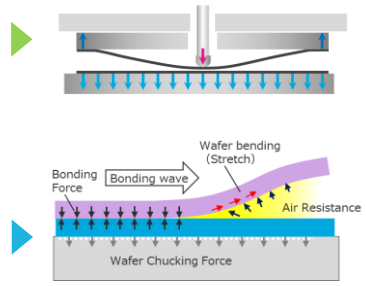


Establishing effective correction to warpage wafer

Distortion Challenges and Actions



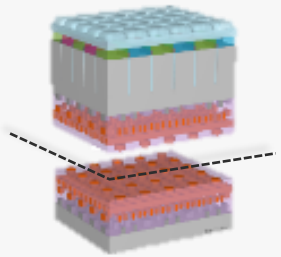
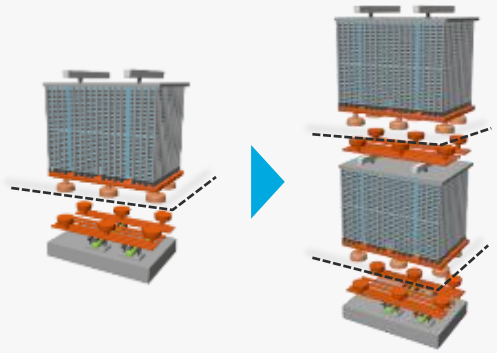
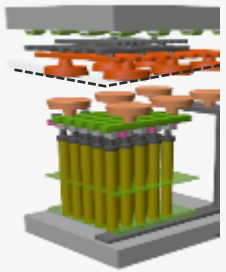
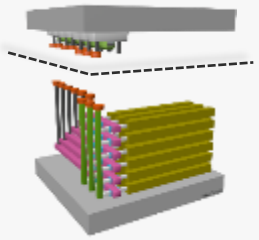
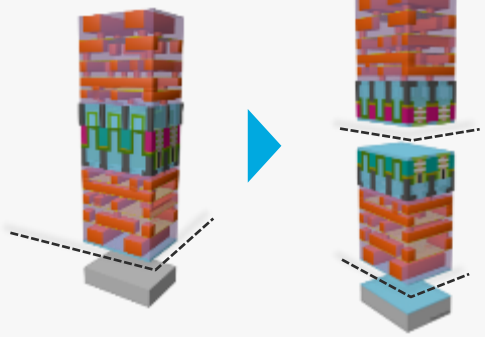
Distortion vector



Optimizing hardware and process

TEL is developing various technologies in advance to prepare for next-generation devices

Broad Applications and Expansion of Bonding Technology

Application	Frontend Process				
	CIS[*1]	NAND	DRAM		Logic
Stacking Device	BSI[*2] Pixel + (Peripheral) + Logic	3D NAND Cell + Peripheral ⋮ + Cell + Cell + Peripheral	VCT[*5] DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	3D DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	BSPDN Logic + Si Substrate BSPDN & CFET Logic + Logic + Si Substrate
Bonding	Wafer to Wafer (CHB[*3]/Fusion)	Wafer to Wafer (CHB)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)
Structure					
Status	HVM[*4]	R&D~HVM / R&D	R&D	R&D	R&D~HVM / R&D

The design of future devices is transitioning from single bonding to multi-bonding structures

*1 CIS: CMOS Image Sensor
*2 BSI: Backside Illumination
*3 CHB: Cu Hybrid Bonding
*4 HVM: High Volume Manufacturing
*5 VCT: Vertical Channel Transistor

TEL

Broad Applications and Expansion of Bonding Technology

Source of all drawings: TEL

Application	Advanced Packaging		
	Stack Memory / HBM	3DIC	
Stacking Device	DRAM Wafer ⋮ DRAM Wafer + DRAM Wafer + Logic Wafer OR DRAM (Die) ⋮ DRAM (Die) + DRAM (Die) + Logic Wafer	SoC Disaggregation Device A Wafer + Device AorB Wafer OR A, B → Die → C → Wafer	Heat Spreader Heat Spreader + Device
Bonding	Wafer to Wafer / Die to Wafer (CHB/Fusion)	Wafer to Wafer / Die to Wafer (CHB)	Wafer to Wafer (Fusion)
Structure	Micro Bump → Change → *Cu hybrid* (More stacks) ▪ Thinner die / more stacks ▪ High density connection ▪ Better thermal conductance Cu	Monolithic SoC (SRAM, CPU/GPU, I/O&Peripheral) → Change → *3D Stack IC* (CPU/GPU) ▪ Small formfactor (3D stack vs. 2D) ▪ Higher speed (shorter wiring, no bump) ▪ Lower power (shorter wiring, no bump) ▪ Lower cost (higher yields, easy to mix processes) ▪ Shorter time to market (matured IP block reuse)	Heat Spreader ▪ Better thermal conductance
Status	R&D	R&D ~ HVM	HVM

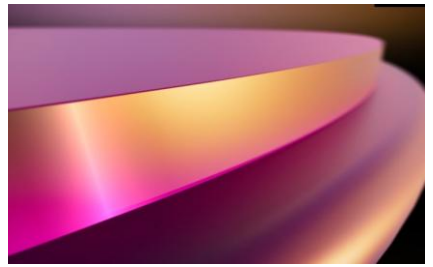
The opportunity for CHB/fusion bonding is growing to encompass advanced packaging

TEL

Laser Trimming System: Ulucus™ L

Source of all drawings: TEL

- **Concept**
  - Edge trimming of bonded wafer with laser
  - Latest platform utilizing super clean technology from frontend process, with the integration of laser control technology
- **Features**
  - High accuracy: enabling narrower trimming width and smooth sidewall with less damage and good yield
  - High-productivity, high-reliability process
  - Environmentally-friendly process by reducing DIW usage by 70% or more



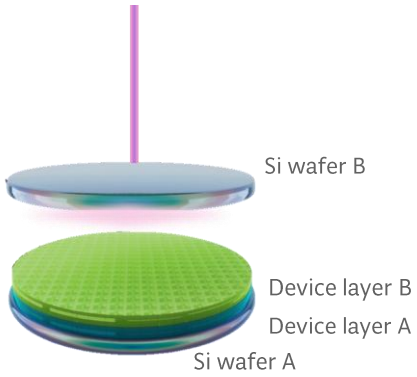
High-accuracy and high-quality laser trimming process - environmentally-friendly and innovative approach for wafer-level bonding

Introducing Ulucus™ LX for Post-Wafer Bonding Process

Source of all drawings: TEL

Extreme laser lift-off (XLO) technology

- Advanced thinning and critical technology for post-wafer bonding process
- Unique laser technology enables separation of the Si-substrate from the device layer



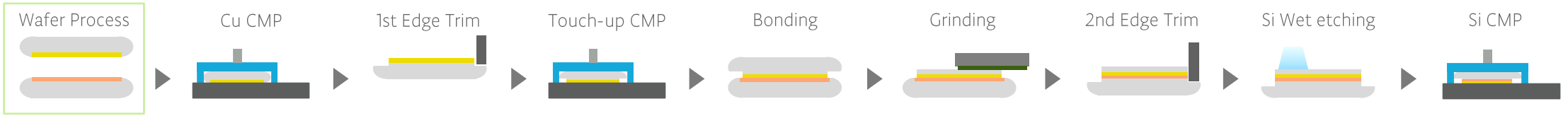
Advantages for process and environment

- Enhanced efficiency in silicon active areas
- Fewer process steps required
- Reduced need for DI water usage and CO_2 emission
- Opportunity for wafer reuse

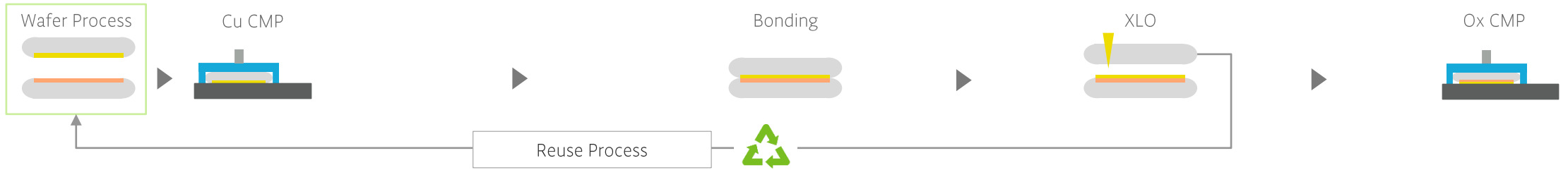
Ulucus™ LX Advantages

Source of all drawings: TEL

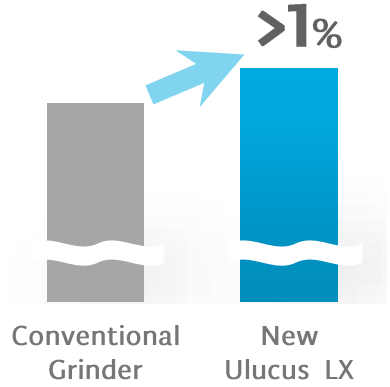
Permanent Bonding Process with Grinding & Blade Edge Trimming (Conventional)



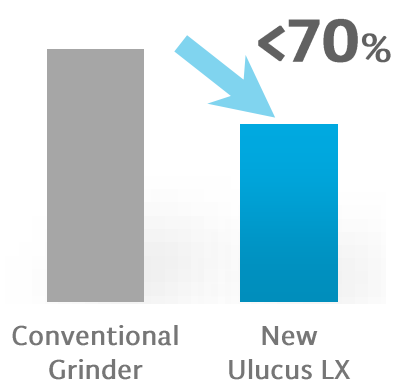
Permanent Bonding Process with XLO (Extreme Laser Lift Off)



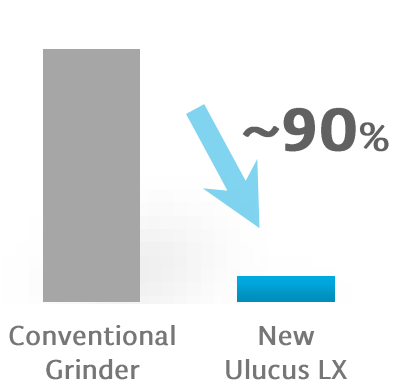
Active Silicon Area



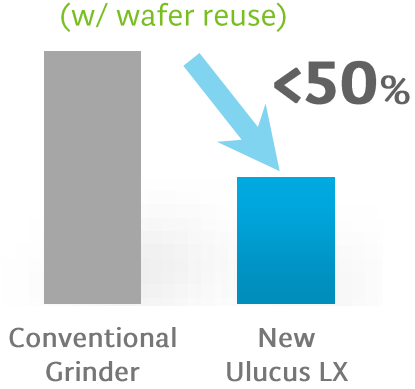
of Process Steps



DIW* Usage



CO_2 Emission (w/ wafer reuse)



No Silicon Sludge

→ Advantage Over Grinder

Source: TEL

* DIW : De-ionized Water

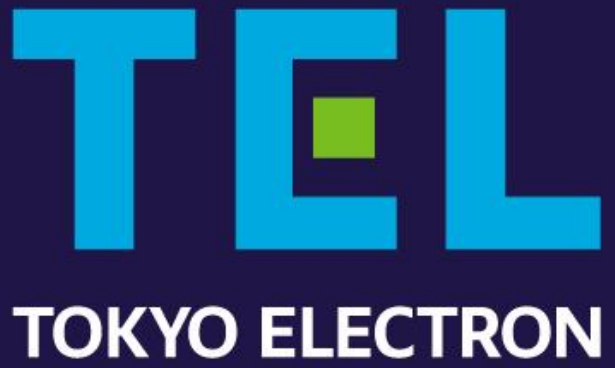

Technology
Enabling
Life

Q&A Session

Closing Remarks

Sam Nakama

President
Tokyo Electron Taiwan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